linear mode. To increase the degree of depletion for a given drain-to-source bias, the source contact (SOURCE) is extended opposite the transition region **710** and is insulated and spaced therefrom by a relatively thin insulating layer (e.g., oxide layer). During on-state operation, the reverse bias established across the metal-insulator-semiconductor (MIS) junction between the source contact extension and the transition region **710** will and induce further depletion of the transition region **710**.

Referring now to FIG. **10**, another preferred UMOSFET device **800** will be described. This device **800** is similar to the device of FIG. **3**, however, a portion of the trench oxide extending between the buried source electrode in the trench and the transition region **810** is thinned in order to increase the degree of coupling between the buried source electrode and the transition region **810** and thereby increase the rate at which the transition region **810** becomes depleted as the drain-to-source voltage is increased during forward on-state operation. As illustrated by FIG. **10**, the UMOSFET device **800** includes an N+ substrate layer **804** (e.g., drain contact layer), a drain electrode **802** and a drift region **806** which may have a graded doping profile therein. A P-type base region **818** is also provided between the transition region **810** and a source region **820**. A highly doped base region extension **814** is also provided, as illustrated. This base region extension **814** operates in combination with the buried source electrode in the trench to deplete the transition region **810** fully before the inversion-layer channel in the base region **818** becomes pinched off (i.e., before it exits the linear mode).

Referring now to FIG. **11**, another preferred vertical device **900** having a lateral MOSFET therein will be described. This device **900** is similar to the device of FIG. **5**G, however, a portion of the trench oxide extending between the source electrode **924** in the trench and the transition region **910** is thinned in order to increase the degree of coupling between the buried source electrode **924** and the transition region **910**. As illustrated by FIG. **11**, the device **900** includes an N+ substrate layer **904** (e.g., drain contact layer), a drain electrode **902** and a drift region **906** which may have a graded doping profile therein. A P-type base region **918** is also provided, as illustrated. A source region **920** and a channel region extension **922** (shown as N+) may also be provided. The source region and channel region extension **922** may be self-aligned to the gate electrode (GATE) using conventional CMOS fabrication techniques.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

That which is claimed is:

1. A vertical power device, comprising:

an insulated-gate field effect transistor that utilizes an N-type transition region in a forward on-state current path extending between a source electrode and a drain electrode of the power device in combination with a P-type base region that forms a P-N rectifying junction with the N-type transition region and a trench-based source electrode that extends in a trench having a sidewall that defines an interface with a vertical first conductivity type drift region of the power device, as means for achieving a forward on-state mode of operation in the power device that simultaneously supports linear operation in an inversion-layer channel of the field effect transistor and velocity saturation operation in the drift region when the drain region is positively biased relative to a source region and the P-N rectifying junction is reversed biased to a point where the N-type transition region, which defines a non-rectifying junction with the N-type drift region, is fully depleted by the P-type base region and a maximum voltage at a drain-side of the inversion-layer channel is less than a gate voltage of the insulated-gate field effect transistor.

2. A vertical power device, comprising:

a semiconductor substrate, said semiconductor substrate comprising an N+ substrate region and an N-type drift region that extends on said N+ substrate region and is more lightly doped than said N+ substrate region;

a P-type base region that extends in said semiconductor substrate and defines a first P-N rectifying junction with the N-type drift region;

an N-type transition region that extends in said semiconductor substrate and defines a non-rectifying junction with the N-type drift region and a second P-N rectifying junction with said P-type base region;

an N+ source region that extends in said P-type base region and forms a third P-N rectifying junction with said P-type base region;

an insulated gate electrode that extends on said semiconductor substrate and is positioned opposite said P-type base region so that application of a sufficiently positive gate voltage to said insulated gate electrode causes formation of an inversion-layer channel that extends in said P-type base region and electrically connects said N+ source region to said N-type transition region;

a trench that extends in said semiconductor substrate and has a sidewall that defines an interface with the N-type drift region;

an insulated source electrode in said trench;

a source electrode that is electrically coupled to said N+ source region;

a drain electrode that is electrically coupled to the N+ substrate region; and

wherein said P-type base region is doped at a sufficiently high level and has a sufficient depth in said semiconductor substrate and a length of the inversion-layer channel is sufficiently short that a depletion region formed at the second P-N rectifying junction pinches off said N-type transition region at an operating point when the inversion-layer channel possesses linear behavior and the N-type drift region possesses velocity saturated behavior when a forward on-state current is present in the inversion-layer channel and the N-type drift region.

3. The power device of claim **2**, wherein the second P-N rectifying junction pinches off said N-type transition region at a point when a maximum voltage at a drain-side of the inversion-layer channel is less than the positive gate voltage.

4. The power device of claim **3**, wherein a maximum N-type doping concentration in said N-type transition region is greater than about ten times an N-type drift region doping concentration at the non-rectifying junction.

5. A vertical power device, comprising:

a semiconductor substrate, said semiconductor substrate comprising an N+ substrate region and an N-type drift region that extends on said N+ substrate region and is more lightly doped than said N+ substrate region;